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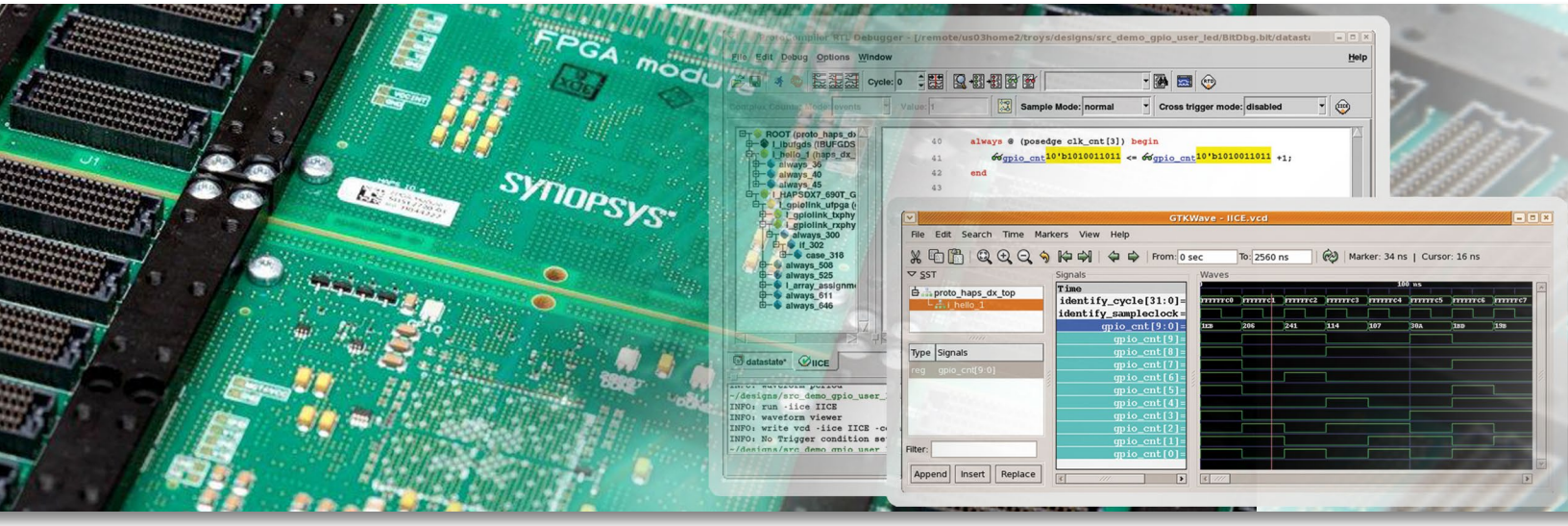
Silicon to Software™



Synopsys' HAPS-70 FPGA-based Prototyping Solution

- High-Speed Time-Domain Multiplexing and Enhanced HapsTrak 3 Connector Deliver Ultra Fast Prototype Performance
- Modular System Architecture Scales from 12 to 288 Million ASIC Gates
- Accelerate Multi-FPGA Partitioning by up to 10X
- Enhanced Universal Multi-Resource Bus Host Connectivity of up to 400MB/s
- Deep Trace Debug Increases Signal Tracing Capacity by 100X
- Compatible with DesignWare IP Prototyping Kits

Overview

Today's ASIC IP and SoC design teams face the dual challenge of very short delivery schedules and high risk of their product being rejected by the market if chip designs ship with defects. Synopsys' FPGA-based prototyping solution enables a more parallel hardware/software development strategy where software developers, validation engineers, and system integration experts have access to prototypes running at near real time speed months before tape-out of new ASIC silicon. FPGA-based prototypes are ideal for pre-silicon software development, system validation, and hardware/software integration of ASIC IP and SoC designs. Prototyping teams benefit from an easy-to-use flow from ASIC RTL to the FPGA-based prototype, high debug visibility, and a scalable hardware architecture to support and streamline IP and SoC system level validation. Synopsys' High-Performance ASIC Prototyping System HAPS®-70 with Symmetrical System Architecture (SSA) offers the best system performance, reliability, and design automation in the industry.

- Enhanced HapsTrak 3 I/O connector technology with high-speed time-domain multiplexing delivers up to 3x performance improvement in data throughput over traditional pin multiplexing
- Modular system architecture scales from 12-288M ASIC gates to accommodate a range of design sizes, from individual IP blocks to processor sub-systems to complete SoCs
- Design planning tools reduce time-to-prototype by 2-3 months streamlining transition from block level IP validation to full system integration
- Synopsys ProtoCompiler's FPGA logic synthesis and automated partition engine for HAPS accelerates time to first prototype from weeks to a single week for a typical 48 million ASIC gate design
- Enhanced Universal Multi-Resource Bus (UMRBus) host connectivity of up to 400MB/s facilitates debug and increases hybrid prototyping performance with Synopsys Virtualizer Development Kits (VDKs)
- Pre-validated Synopsys DesignWare IP with HAPS systems enables efficient integration of small IP blocks and earlier software development
- Eliminate RTL flaws fast with simulator-like debug visibility across multiple-FPGAs and deep trace storage of up to 8GB

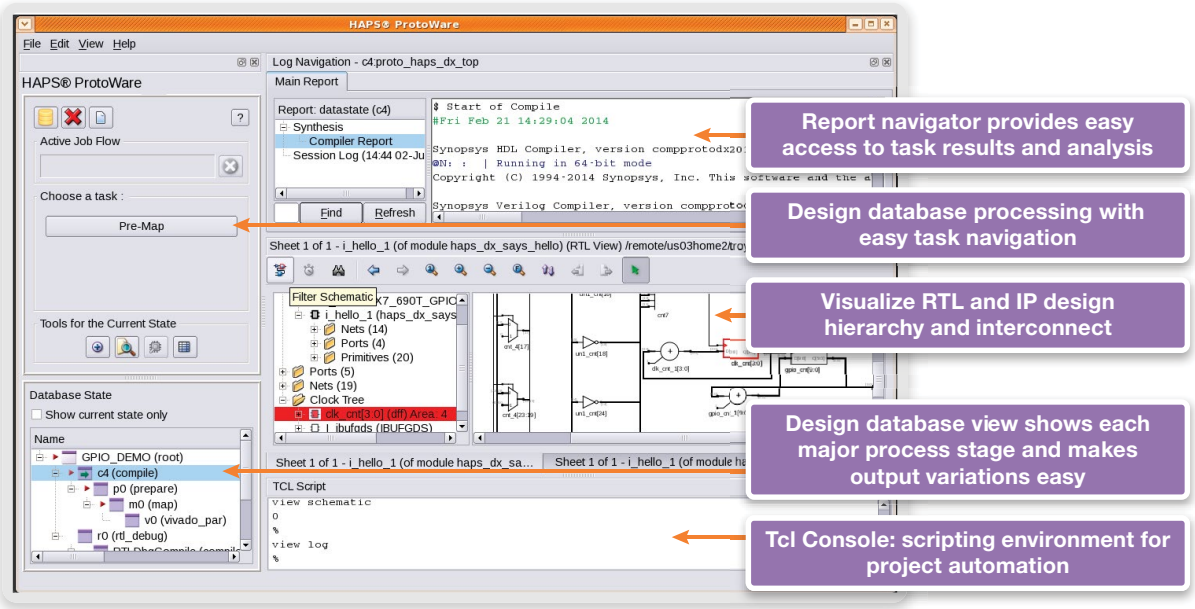


Figure 1: HAPS-Aware Prototyping Planning with ProtoCompiler

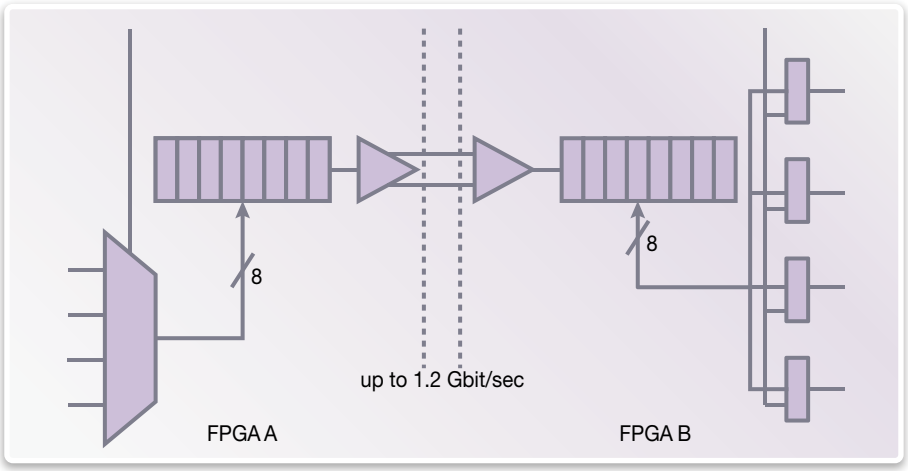


Figure 2: High-Speed Time-Domain Multuplexing (HSTDM)

The HAPS-70 Symmetrical System Architecture (SSA) is designed to provide a near seamless integration path for single-FPGA IP module to be integrated into a system of multi-FPGA SoC modules maximizing prototype reuse across engineering teams. SSA enables a bottom-up ASIC-like design flow for high-capacity FPGA-based prototypes by allowing lower capacity HAPS-70 design project constraints and optimization options to be reused in the context of a higher capacity target. This modular approach is enabled by the mechanical symmetry of the PCB and connector layout of the HAPS-70 system and project flows automated by the Synopsys ProtoCompiler design and debug environment for HAPS. In both IP and SoC usage modes, the solution delivers unparalleled performance, ease of use, debug visibility, and system control.

A fully automated partition and system route engine eliminates pin congestion while maximizing performance with high-speed time-domain multiplexing (HSTDM) tailored for the HAPS system hardware.

Easy to Use Flow from RTL to Prototype

ASIC/SoC designs can be a challenge to prepare for an FPGA-based prototype. There are several conversions necessary and always the potential for overflowing FPGA I/Os. The automation features of Synopsys ProtoCompiler help maximize your productivity and create prototypes with the best system performance.

The ProtoCompiler software with HAPS System awareness delivers an integrated flow which is easy to use and automates SoC RTL to FPGA-based prototype bring-up. ProtoCompiler features address the needs of the FPGA-based prototyping engineer including system definition of the target resources (FPGAs, memories, connectors, and other physical interfaces), ASIC clock conversion, design planning across multiple FPGAs, eliminating I/O congestion between FPGAs, library and IP conversion, FPGA implementation, and system-level static timing analysis. With its HAPS system awareness, ProtoCompiler is able to automate many of the steps which were traditionally completed manually.

FPGA logic synthesis for HAPS provides dedicated HDL compilers and optimization tuned to your objective whether it's short bring-up time or high system performance. A high capacity, constraint-driven, partition engine solves the most difficult partition problems for ASIC designs that require multiple FPGAs to prototype. ProtoCompiler can generate a fit solution for a 4 FPGA, 48 million ASIC gate design in under 10 minutes.

Prototype projects developed for HAPS-DX or HAPS-70 Series systems are directly compatible and allow you to integrate individual IP prototype projects into larger subsystems for full SoC validation, and automate repetitive tasks and project processing with the Tcl command interface.

All of the HAPS-70 I/O's are HSTDM capable delivering faster convergence on a partitioning solution while maximizing system performance.

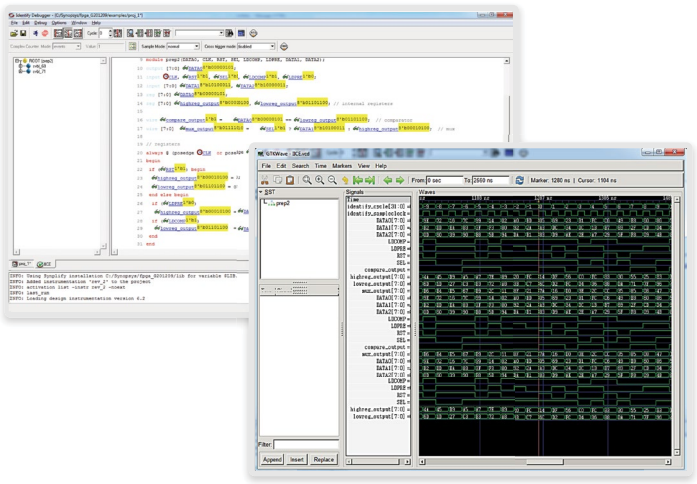


Figure 3: Simulator-Like Signal Browsing with ProtoCompiler's RTL Debugger

Greater Debug and Prototype Bring-Up Tools With Fast Turnaround

FPGA-based prototyping hardware has evolved from external logic analyzers to embedded probes to view activity at the post-synthesis gate-level. Design debug is hard from the gate/chip-level perspective and a multi-FPGA prototype compounds the debug problem by splitting design elements across FPGAs. Finding problems is easier if you're able to instrument data signals and debug from the RTLsource perspective and can seamlessly view results across FPGAs.

The HAPS-70 systems with ProtoCompiler's debug features provide an array of debug capabilities which can be deployed at any stage of the ASIC prototyping project ensuring that the source of a design bug can be located as fast as possible. The HAPS Aware debug capabilities integrate seamlessly and non-intrusively into the design and provide simulator-like visibility of the prototyping project at RTL source level. The design can be debugged irrespective of the prototype partition with seamless multi-FPGA debug visibility. With HAPS Deep Trace Debug enhanced visibility into the design, users have as much as 8GB of sample storage by utilizing off-chip, external memory storage. Sample results are available quickly over the high-performance HAPS Universal Multi-Resource Bus (UMRBus) Interface Pod link between the debugger workstation and the HAPS-70 system.

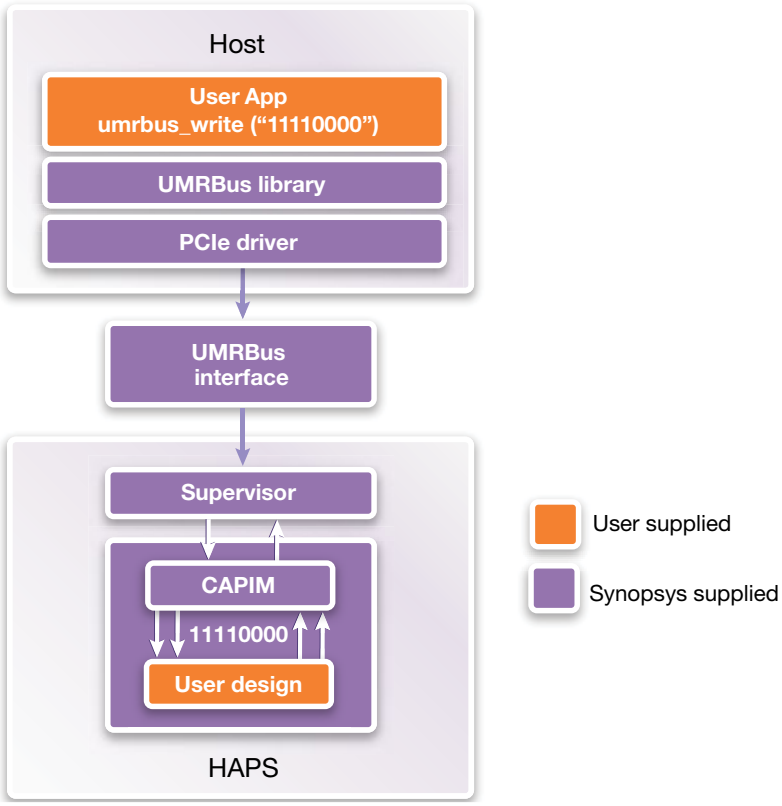


Figure 4: High-performance communication for HAPS via UMRBus API

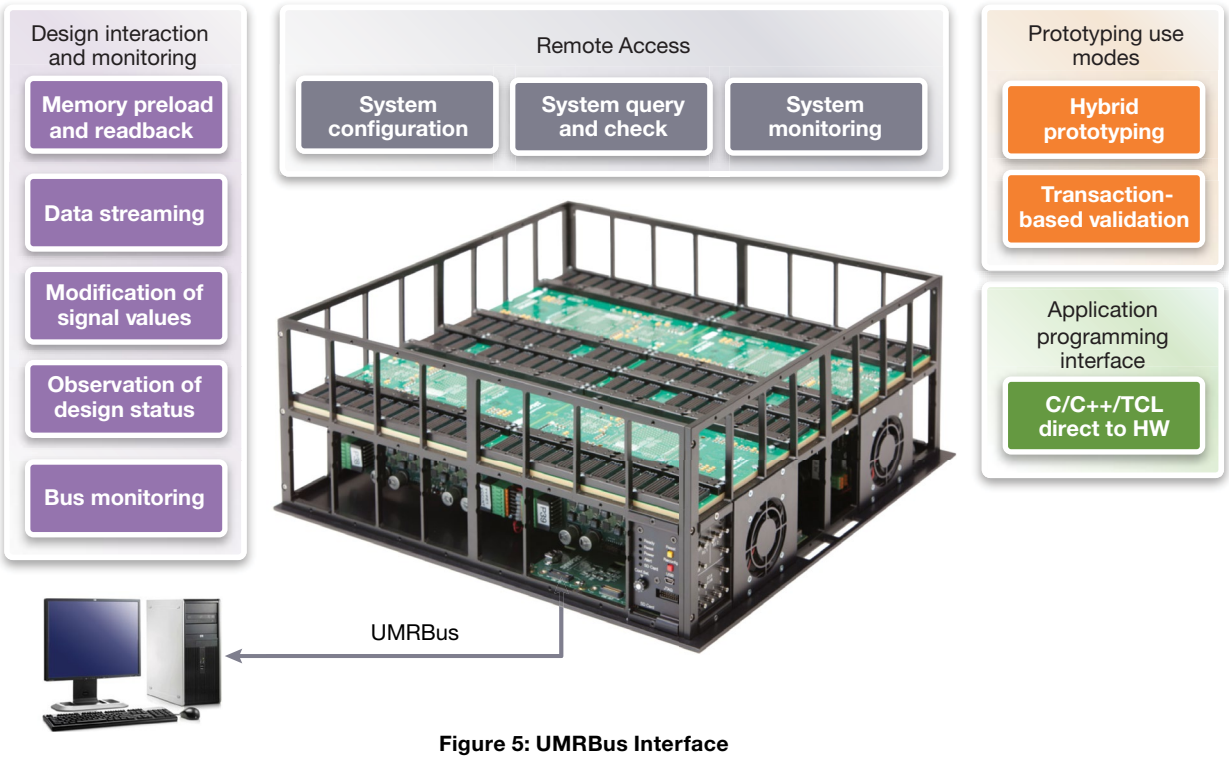


Figure 5: UMRBus Interface

The creation of user defined bus monitors and protocol checkers is simplified by leveraging the automated flow, non-intrusive and zero pin overhead of the UMRBus Client Application Interface Modules (CAPIMs). These UMRBus RTL building block modules provide the basis of user defined debug to stimulate and monitor modules that enable the user to interact with the HAPS-70 system through the provided UMRBus application programming interface. This API enables design interaction via simple TCL or the building of more complex analysis tools via the C++ documented interface.

High Performance System for Software Development and System Validation

The integrated solution of ProtoCompiler software and HAPS-70 systems produces high performance and accurate (high fidelity) IP or SoC level prototyping models capable of running at near real world speeds utilizing real world I/O. ProtoCompiler's HAPS-70 aware multi-FPGA prototyping software enables key customizations and performance optimizations such as the insertion of high-speed time-domain multiplexing (HSTDM).

This higher performance ensures realistic application level software development exercised by real world I/O. Even with greater FPGA capacity, SoC designs typically need to be partitioned across multiple FPGA's leading to the problem of passing sometimes thousands of design block signals between FPGA's. HSTDM is Synopsys's unique capability for packing up signals and transmitting them between FPGA's at very high performance. When pin multiplexing is required the HAPS-70 and HSTDM capability provide 3X or more performance improvement when compared to traditional pin multiplexing solutions.

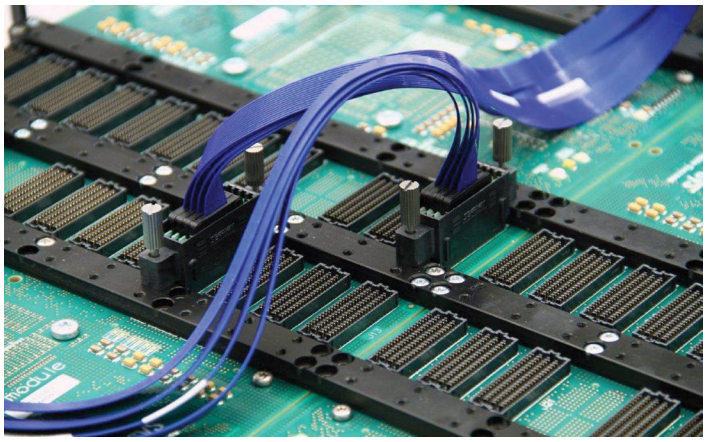


Figure 6: High-Speed HapsTrak 3 Connector Technology

High Performance Features Include:

- Enhanced FPGA-Module for high-speed signaling
- HapsTrak 3 connector technology with significant performance improvements making it easy to support high performance I/O interfacing to components such as DDR3-1333
- High-performance HapsTrak 3 interconnect cables for highspeed interconnectivity between FPGAs and systems
- Access to sixteen multi-gigabit channels per Xilinx® Virtex®-7 2000T FPGA providing direct access to high speed transceivers
- Improved system stability with advanced power and thermal management

Flexible and Scalable to Support IP and SoC Designs

The HAPS-70 systems support both IP and SoC level prototyping tasks including software development, system validation and customer demonstrations at near real time speeds with real world I/O. Capacity scalable systems support configurations from 12 million to 288 million ASIC gates. Realize close to seamless integration of IP level prototypes into larger SoC level prototypes when utilizing the HAPS-70 systems with the optimized ProtoCompiler software flow. Designs targeting smaller HAPS systems can be easily migrated to the larger HAPS systems. The HAPS-70 Symmetrical System Architecture (SSA) ensures pin-to-pin forward compatibility for constraints and physical connections such as cables and daughter boards. The SSA architecture facilitates the easy movement of prototyping designs, cable connections, and daughter boards. Each bank of connectors has delay matched characteristics ensuring minimum impact to timing when components need to be moved. The HAPS-70 IP prototyping FPGA images can be used standalone for IP validation and quickly integrated into SoC prototypes increasing reuse opportunities while reducing effort and accelerating SoC validation. opportunities while reducing effort and accelerating SoC validation.

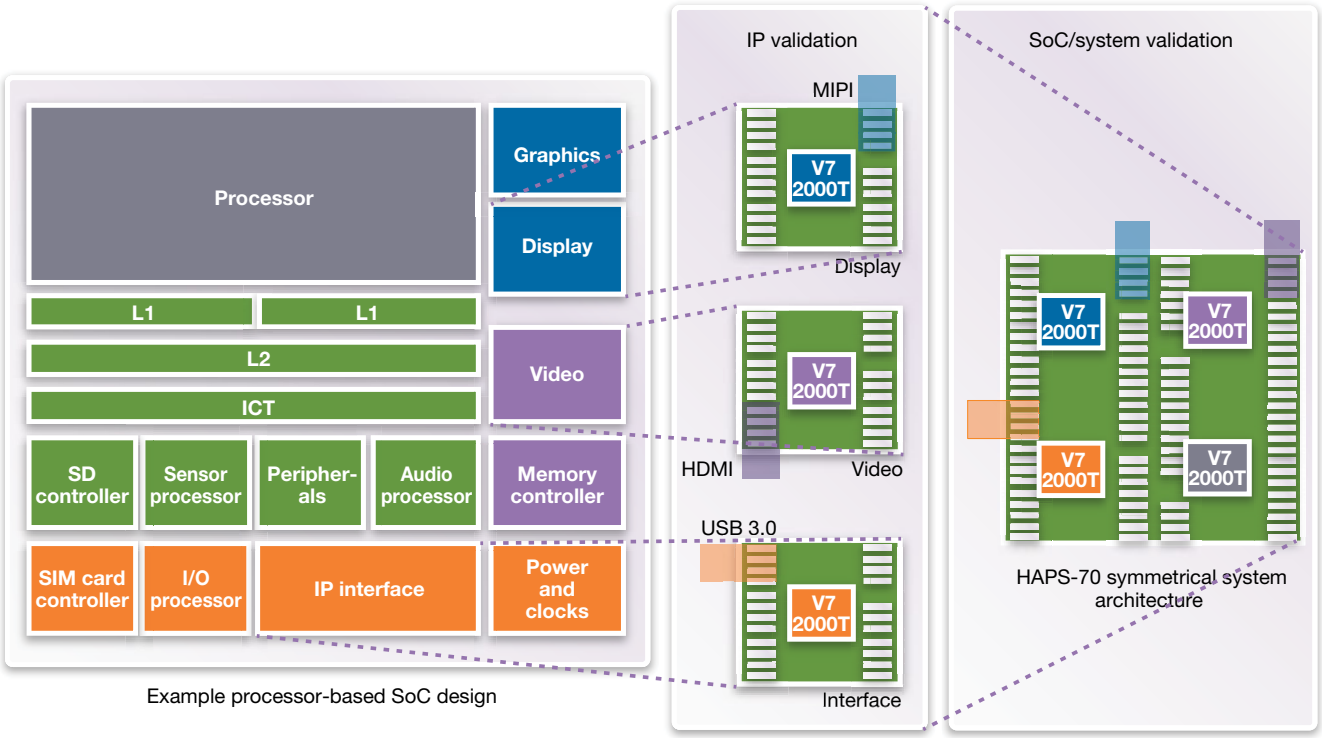


Figure 7: HAPS-70 Symmetrical System Architecture for IP and SoC Prototyping

	HAPS-70 S12	HAPS-70 S24	HAPS-70 S36	HAPS-70 S48	HAPS-70 S60	HAPS-70 S72	HAPS-70 S96	HAPS-70 S120	HAPS-70 S144	Custom Configuration
FPGA Type	Virtex-7 XC7V2000T									
Number of FPGAs	1	2	3	4	5	6	8	10	12	Up to 24
ASIC Gate Capacity	Up to 12M	Up to 24M	Up to 36M	Up to 48M	Up to 60M	Up to 72M	Up to 96M	Up to 120M	Up to 144M	Up to 288M
I/O Connectors HapsTrak 3	23	46	69	92	115	138	184	230	276	Up to 552
User Accessible I/O Resources	1126	2252	3378	4504	5630	6756	9008	11260	13512	Up to 27024
High Speed I/O Transceivers	16	32	48	64	80	96	128	160	192	Up to 384
Routing Granularity	50 I/Os per connector, variable voltage region (1.8 V, 1.5 V, 1.35 V, 1.2 V) per connector									
Clock Resources	2 PLLs, 2 external PLL inputs, 2x2 external PLL outputs, 2x6 clock input and outputs, frequency range from 5 MHz to 200 MHz, clock stopping support									
Debug Modes	RTL Level Debug, Sample Mux Groups, Multi-FPGA Distributed Debug, Deep Trace Debug									
Daughter Board Portfolio	PCIE Gen 2, SATA, Ethernet, DDR3-1333, DDR2, SRAM, FLASH, MSDRAM, MICTOR									
Prototyping Use Modes	Co-simulation, Hybrid prototyping, native UMRBus, SCE-MI 2.0, C/C++/TCL									
System Control Software	System Configuration and Monitoring software tools Included									
Configuration	JTAG, USB 2.0, Parallel Flash, SD Card, UMRBus via Configuration and Data Exchange (CDE) interface									
Encryption Key	Battery backup support									
Power	110-240 AC, 12V									

Table 1: HAPS-70 Series Features

Figure 8: HAPS-70 Series Prototyping System

HAPS-70 Series Prototyping System

The modular architecture of the HAPS-70 Series allows you to assemble any permutation of 1, 2, or 4 FPGA systems up to 24 total FPGAs, supporting up to 288 million ASIC gate designs. The “ASIC” like design flow supports modular and incremental compilation reducing the number of iterations between each RTL code cycle. ProtoCompiler delivers prototyping optimized modes such as “fast” and “continue-upon error” modes to reduce iterations required for system bring-up, capable of identifying multiple errors in one synthesis run. Easier system build up is achieved utilizing the HAPS-70’s portfolio of available off-the-shelf daughter boards, cables and accessories. Users can reduce custom daughter board development effort by leveraging Synopsys’s large portfolio of cables, connectors and daughter boards including HapsTrak 3 native daughter boards such as, LAB I/O, DDR3, SRAM. Users can leverage most of the existing Synopsys portfolio of daughter boards and reuse custom built HapsTrak daughter boards utilizing the HapsTrak adapter. Direct PCIE, SATA and Ethernet connectivity supported by multi-gigabit daughter boards are also available from Synopsys.

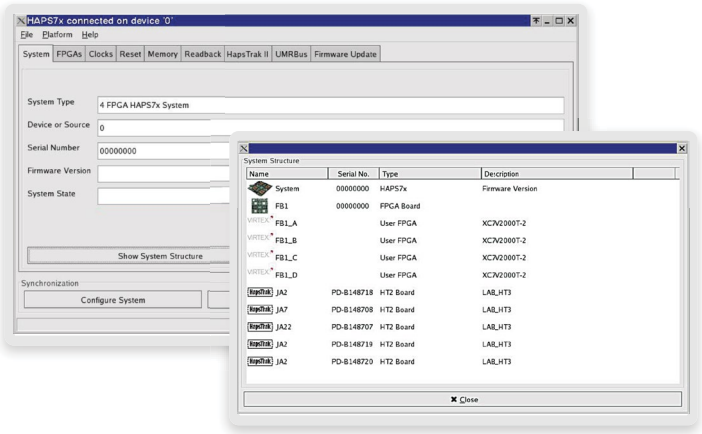


Figure 9: Integrated System Utility GUI Interface

Worry-Free Setup and Integrated System Check Utility

To ease the system bring-up phase, the HAPS-70 series systems are used with a worry-free setup utility including:

- Graphical user interface for ease of use and TCL interface for scriptable configuration
- Automated handling of clock and reset distribution
- Automated thermal management `Shutdown protocols protecting your investment
- Fast configuration and FPGA programming over UMRBus
- A hassle free, stable and reliable operation each time
- A system check ensuring cables, daughter boards, and system configuration setup match the prototyping design database
- A system performance analyzer that profiles the physical connections on the system ensuring the desired cable connector or HSTDM connection performance is met

HAPS-70 Prototyping System Highlights

- Support for IP and SoC Designs up to 288M ASIC gates
- New HapsTrak 3 connector technology for high speed I/O interfaces
- Modular and scalable architecture from 1 to 24 FPGAs
- Highest flexibility with 1126 user accessible I/Os per FPGA module
- Unique low latency host system communication for highspeed data transfer

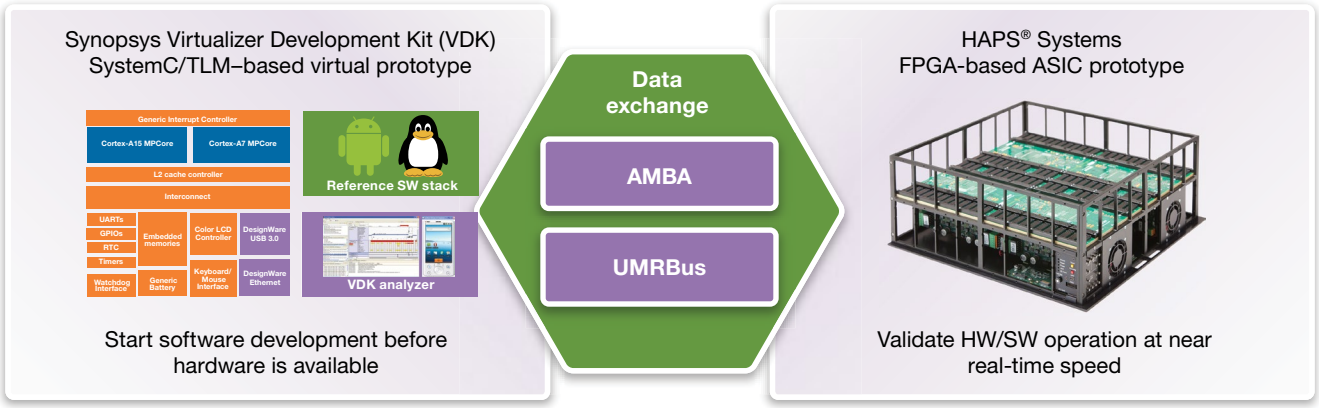


Figure 10: Hybrid Prototyping Solution

Start HW/SW Validation and Software Development Earlier

The HAPS-70 system supports Synopsys' Hybrid Prototyping, DesignWare IP capabilities enabling HW/SW validation and software development to start earlier in the product development process. Hybrid Prototyping offers an out-of-thebox solution seamlessly integrating Synopsys VDK virtual prototypes and HAPS FPGA-based Prototyping to accelerate SoC software and hardware development. Users benefit from the best of both worlds by seamlessly linking virtual and FPGA-based prototypes together. Hybrid prototyping combines the accuracy and speed of HAPS with the flexibility and visibility of a VDK.

Partition SoC design blocks at the logical AMBA bus interface level between virtual and FPGA-based environments to maximize the overall prototyping performance and easily integrate all design blocks into a single hybrid prototype including high performance ARM® Cortex processor virtual TLM-2.0 based models, Transactors for ARM AMBA® interconnect, and DesignWare IP. The enhanced UMRBus is capable of supporting up to 400 MB/s of high speed connectivity to ensure a high performance and very low latency link between virtual prototypes and HAPS FPGA-based prototyping systems.

Compatible With HAPS-DX and DesignWare IP Prototyping Kits

HAPS-DX Plug and play compatibility with HAPS-70 allows you to integrate multiple single-FPGA protoyping projects for full subsystem or SoC validation scenarios. Chain multiple HAPS-DX systems with a HAPS-70 system as a "master" controller. Synopsys also offers assistance to customize DesignWare IP subsystems for specific application requirements or target the HAPS-70 series for prototyping scenarios.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.

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